CLAIMS

What is claimed is:

1. A System-On-Chip (SOC) architecture comprising:
a system bus;
a processor in communication with the system bus;
an input/output (I/O) interface in communication with the system bus; and
a ferroelectric memory component in communication with the system bus.

2. The SOC of claim 1, further comprising debugging and self-test modules in communication with the system bus.

3. The SOC of claim 1, further comprising a direct memory access (DMA) component in communication with the system bus.

4. The SOC of claim 1, further comprising a memory controller in communication with the system bus.

5. The SOC of claim 1, further comprising re-configurable hardware in communication with the system bus.

6. The SOC of claim 5, wherein the re-configurable hardware has a ferroelectric memory component embedded therein, and wherein the re-configurable hardware has a configuration that is stored in the ferroelectric memory component embedded in the re-configurable hardware.

7. The SOC of claim 5, wherein the ferroelectric memory component embedded in the re-configurable hardware is a ferroelectric random access memory (FeRAM) component.

8. The SOC of claim 1, wherein the ferroelectric memory component is a ferroelectric random access memory (FeRAM) component.

9. The SOC of claim 1, wherein the processor is a microprocesssor.

10. The SOC of claim 1, wherein the processor is a microcontroller.

11. The SOC of claim 1, wherein the ferroelectric memory component stores programs and data needed by the processor for execution of the programs by the processor, and wherein, during execution of a program by the processor, the processor causes an instruction pointer to be stored in a predetermined location in the ferroelectric memory component that identifies a location in the ferroelectric memory component that contains an address of a next instruction to be executed by the processor.

12. The SOC of claim 11, wherein the SOC comprises a re-configurable hardware component in communication with the system bus, and wherein the processor causes the configuration of the re-configurable hardware component to be stored in the ferroelectric memory component.

13. The SOC of claim 12, wherein when the re-configurable hardware is executing, current state values of the re-configurable hardware are stored at predetermined locations in the ferroelectric memory component, and wherein if a power cycle occurs, then when power returns, the processor uses the instruction pointer to obtain the next instruction to be executed and resumes execution of the program.

14. The SOC of claim 13, wherein if a power cycle occurs, when power returns, said current state values are read out of the ferroelectric memory component and used by the re-configurable hardware to resume execution of the re-configurable hardware.

15. The SOC of claim 1, further comprising an intellectual property (IP) hardware component in communication with the system bus.

16. The SOC of claim 15, further comprising an input/output (I/O) hardware component in communication with the system bus.

17. The SOC of claim 16, further comprising a static random access memory component.

18. The SOC of claim 17, further comprising a dynamic random access memory (DRAM) component.

19. A method for preventing an occurrence of a power cycle in a System-On-Chip (SOC) architecture from requiring that the SOC be rebooted and re-initialized, the method comprising the steps of:

storing, in a ferroelectric memory component embedded in the SOC, an address pointer to an address location in the ferroelectric memory component that contains a next instruction to be executed by a processor embedded in the SOC, said next instruction being part of an instruction set currently being executed by the processor;

after a power cycle has occurred, when power returns, accessing by the processor said next instruction, the processor using the address pointer to access said next instruction; and

executing, in the processor said next instruction, thereby resuming execution of the instruction set.

20. The method of claim 19, wherein the ferroelectric memory component is a ferroelectric random access memory (FeRAM) component.

21. The method of claim 19, wherein the SOC has re-configurable hardware embedded therein, and wherein the method further comprises the step of:

prior to the occurrence of the power cycle, storing a configuration of the re-configurable hardware and current state of the re-configurable hardware in the ferroelectric memory component.

22. A computer program for use in a System-On-Chip (SOC) architecture, the computer program being embodied on a computer readable medium, the program comprising:

a first code segment for storing, during execution of an instruction set, an address pointer in a ferroelectric memory device, the address pointer pointing to a location in the ferroelectric memory component that contains a next instruction of the instruction set to be executed; and

a second code segment for utilizing the address pointer to access the location in the ferroelectric memory component that contains said next instruction, said second segment being executed after a power cycle has occurred.